UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,549	11/28/2003	Kuo-Jeng Wang	4425-337	9088

43831 7590 11/19/2007

BERKELEY LAW & TECHNOLOGY GROUP, LLP
17933 NW Evergreen Parkway, Suite 250
BEAVERTON, OR 97006

EXAMINER	
SUAREZ, FELIX E	
ART UNIT	**PAPER NUMBER**
2857	

MAIL DATE	DELIVERY MODE
11/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/722,549	WANG ET AL.	
	Examiner	Art Unit	
	Felix E. Suarez	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-11 and 14-19 are rejected under 35 U.S.C. 102(b) as being unpatentable over Vo-Dinh et al. (U.S. Patent No. 6,197,503).

With respect to claims 1 and 14, Vo-Dinh et al. (hereafter Vo-Dinh) teaches a biosensor with multi-channel A/D conversion (or a method for determining a content of a specific component of a specimen), comprising:

a chip (300, 302, 306 in combination, FIG. 13) generating a time-dependent analog signal in response to a content of a specific component of a specimen provided on said chip (see col. 8, lines 1-7, highly integrated biosensors are made possible party through the capability of fabricating multiple optical sensing elements and microelectronics on a single integrated circuit (IC); and see col.10, lines 51-61, in a partially parallel readout scheme, a row of diodes are multiplexed into one amplifier/low pass filter circuit. The output of each filter is input to a multi-channel analog-to-digital converter (ADC), which can be implemented on the same IC as the photodiode array, amplifier and filter.

Compared to the sequential or serial readout case, the time required is reduced by a factor of n for an nxn array);

a multi-channel A/D converter (see col. 10, lines 51-57, input to 304 FIG. 13. multi-channel analog-to digital converter) with multiple channels each of which simultaneously receiving the time-dependent analog signal in each sampling interval in order that said multi-channel A/D converter converts the time-dependent analog signal to a set of digital signals (see col.10, lines 51-61, in a partially parallel readout scheme, a row of diodes are multiplexed into one amplifier/low pass filter circuit. The output of each filter is input to a multi-channel analog-to-digital converter (ADC), which can be implemented on the same IC as the photodiode array, amplifier and filter. Compared to the sequential or serial readout case, the time required is reduced by a factor of n for an nxn array); and

a microprocessor (see col. 1, lines 25-28, microprocessor chips or micro-electro-mechanized system) receiving the sets of digital signals in a period of sampling time and determining the content of the specific component based on the sets of digital signals (see col. 1, lines 25-28, microprocessor chips, and see col. 6, lines 20-23, micro-electro-mechanized system (MEMs)).

With respect to claims 2 and 15, Vo-Dinh further teaches that, the time-dependent analog signal is in a form of response current (see col. 9, lines 24-31, the operational amplifier and feedback resistor form a trans-impedance amplifier

that is used to convert photo-current into a voltage).

With respect to claims 3 and 16, Vo-Dinh further teaches comprising: a current/voltage converter to convert the time-dependent analog signal to a time dependent output voltage prior to sending to said multi-channel A/D converter (see col. 9, lines 24-31, the operational amplifier and feedback resistor form a trans-impedance amplifier that is used to convert photo-current into a voltage).

With respect to claim 4, Vo-Dinh further teaches, said current/voltage converter includes an operational converter (see col. 9, lines 47-50; and FIG. 9, as the operational amplifier output cannot exceed the positive supply, the maximum output will be approximately 5 V, so the maximum signal excursion is 3 V, which corresponds to a maximum current of 3 V/R1).

With respect to claim 5, Vo-Dinh further teaches, said multi-channel A/D converter includes a sampler, a multi-channel converter and a logic circuit (see col. 10, lines 51-61, nxn array sample, multi-channel circuit and analog-to-digital converter).

With respect to claim 6, Vo-Dinh further teaches, said multi-channel A/D converter includes a sampler, a multi-channel converter and a logic circuit (see col. 10, lines 51-61, nxn array sample, multi-channel circuit and analog-to-digital

converter).

With respect to claim 7, Vo-Dinh further teaches, said multi-channel A/D converter includes a sampler, a multi-channel converter and a logic circuit (see col. 10, lines 51-61, nxn array sample, multi-channel circuit and analog-to-digital converter).

With respect to claims 8 and 18, Vo-Dinh further teaches, said microprocessor includes a mapping table of peak value versus content of the specific component, the peak value representing a maximum value of a time-dependent discharge curve constituted by the sets of digital signals collected during the period of sampling time, and said microprocessor determines the content of the specific component in accordance with the mapping table (see col. 20 line 66 to col. 21 line 6; and FIG. 19, the four peaks in FIG. 19 illustrate the detection of the four DNA spots on the substrate by the amplifier/phototransistor Integrated Circuit Microchip (AP- ICM) device).

With respect to claims 9 and 19, Vo-Dinh further teaches, said microprocessor includes a mapping table of peak value versus content of the specific component, the peak value representing a maximum value of a time-dependent discharge curve constituted by the sets of digital Signals collected during the period of sampling time, and said microprocessor determines the

content of the specific component in accordance with the mapping table (see col. 20 line 66 to col. 21 line 6; and FIG. 19, the four peaks in FIG. 19 illustrate the detection of the four DNA spots on the substrate by the amplifier/phototransistor Integrated Circuit Microchip (AP- ICM) device).

With respect to claim 10, Vo-Dinh further teaches, said microprocessor includes a mapping table of rising time versus content of the specific component, the rising time corresponding to a maximum value of a time-dependent discharge curve constituted by the sets of digital signals collected during the period of sampling time, and said microprocessor determines the content of the specific component in accordance with the mapping table (see col. 20 line 66 to col. 21 line 6; and FIG. 19, the four peaks in FIG. 19 illustrate the detection of the four DNA spots on the substrate by the amplifier/phototransistor Integrated Circuit Microchip (AP- ICM) device).

With respect to claim 11, Vo-Dinh further teaches, said microprocessor includes a mapping table of rising time versus content of the specific component, the rising time corresponding to a maximum value of a time-dependent discharge curve constituted by the sets of digital signals collected during the period of sampling time, and said microprocessor determines the content of the specific component in accordance with the mapping table (see col. 20 line 66 to col. 21 line 6; and FIG. 19, the four peaks in FIG. 19 illustrate the detection of the four

DNA spots on the substrate by the amplifier/phototransistor Integrated Circuit Microchip (AP- ICM) device).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vo-Dinh et al. (U.S. Patent No. 6,197,503) in view of Perov et al. (U.S. Patent No. 6,407,395).

With respect to claims 12 and 13, Vo-Dinh teaches all the features of the claimed invention, except that Vo-Dihn does not teach:

comprising a liquid crystal display for displaying a reading of the content of the specific component.

But Perov et al. (hereafter Perov) teaches in a portable biochip scanner device that, the signal is digitized with an analog-to-digital converter (ADC) and processed by a microprocessor board. The processing may include digital filtering and integration of the signal. The microprocessor can also be used as a

driver of a compact liquid-crystal display (LCD) employed for monitoring the scanner output (see Perov; col. 3, lines 40-45).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Vo-Dinh to include a LCD as taught by Perov, because the LCD of Perov allows to display and monitor a scanner output, as desired.

3. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over (U.S. Patent No. 6,197,503) in view of Miyazaki et al. (U.S. Patent No. 7,232,510).

With respect to claim 20, Vo-Dinh teaches all the features of the claimed invention, except that Vo-Dihn does not teach:

comprising a step of establishing a voltage-time discharge curve in accordance with the sets of digital signals collected during the period of sampling time.

But Miyazaki et al. (hereafter Miyazaki) teaches in a biosensor measurement instrument that, the profile shown in FIG. 9, the preprocess starts at time t0 and includes three consecutives periods, the first voltage period is a standby period; and then a quantity of discharged electron increases, and a high response current is thus observed at time t2 (see Miyazaki; col. 14, lines 15-39).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Vo-Dinh to include a biosensor measurement instrument as taught by Miyazaki, because the a biosensor measurement instrument of Miyazaki allows to display a process profile of a voltage-time discharge, as desired.

Conclusion

Prior Art

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kawanaka [U.S. Patent No. 6,349,230] describes a blood measurement instrument.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Felix Suarez, whose telephone number is (571) 272-2223. The examiner can normally be reached on weekdays from 8:30 a.m. to 5:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo Ramos-Feliciano can be reached on (571) 272-7925. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300 for regular communications and for After Final communications.

October 11, 2007

F.S.

ELISEO RAMOS-FELICIANO
SUPERVISORY PATENT EXAMINER